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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

02255396.0

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Circuit for power amplification

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Circuit for power amplification

Technical Field of the Invention

The present invention relates to a power control circuit and method, and in particular to the control of output power of a high frequency power amplifier.

Description of the Related Art

In modern telecommunication systems, radio frequency (RF) power amplifiers are used to control output power of mobile devices (such as cellular telephones, cordless telephones, two-way pagers, wireless LAN, AM/FM analogue transmitters) prior to, and during, signal transmission. These RF power amplifiers typically generate an output power in the range of 50mW to 3W. Known RF power amplifiers can control output power at a RF load (which is generally an antenna) via biasing an output transistor.

Generally in RF power amplifiers, impedance at the output transistor must match the nominal impedance of the load in order to avoid problems such as unwanted standing waves (resulting from signal reflection at the load) in the apparatus. Efficient antenna operation requires that the antenna is matched to the circuit service, to ensure maximum energy transfer. The quality of system matching is measured in terms of a parameter known as voltage standing wave ratio (VSWR). This parameter can be determined for frequencies at which a particular system operates. Optimum operation in a RF power amplifier requires a 1:1 VSWR at all relevant frequencies. Unfortunately, many conventional antennas exhibit a high VSWR (for example, greater than 3:1) which adversely affects efficiency, especially in

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wideband antennas, unless some form of compensatory matching network is used. Use of such compensatory matching networks is undesirable because they tend to decrease transmission power available and slow the operation of the system.

The impedance of a load such as an antenna varies with motion and position and thus, impedance variation is common for mobile devices. The impedance variation results in a voltage swing across the collector electrode of the output transistor of the RF power amplifier. For example, a RF power amplifier driving a cellular telephone antenna with 50 Ohms nominal impedance may, at times, be required to drive a high output transistor impedance, which could lead to a VSWR as high as 20:1.

Substantially mismatched loads (and hence a high VSWR) can lead to a degradation of the RF power amplifier. This degradation, or even transistor failure, occurs as a result of exceeding the collector-emitter voltage and collector current that can safely be applied to a bipolar transistor (here, the output transistor) within the constraints of the 'secondary breakdown' effect.

The output transistor is not able to draw d.c. current (as a capacitor is used to remove the d.c. component) and so the output bias circuitry provides increased bias current, which leads to increased input power to the output transistor. Where a system is experiencing high VSWR and high load impedance, and hence a large voltage swing at the collector electrode of the output transistor, it is possible that negative gain can occur in the output amplifier.

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United States Patent 5,455,968(Pham) discloses a variable power amplifier including a final stage amplification element. This element is coupled to a bias network which aims to provide stability where output mismatch conditions exceed 5:1 VSWR.

Japanese Patent JP 11284522 describes a system to maintain constant output power in a high frequency power amplifier. An output signal of a second amplifier is detected, processed and input to a first amplifier. The system involves the use of a directional coupler.

Therefore, it can be seen that it is desirable to control output power of an RF power amplifier where the impedance of the load is varying.

Summary

According to a first aspect of the present invention, there is provided a method of controlling output from a power amplifier which has a driver stage and an output stage, the method comprising detecting a first and a second electrical parameter at an output of the output stage; processing the first parameter with a first reference signal to generate a bias control signal; processing the second parameter with a second reference signal to generate a bias reduction signal; feeding the bias control signal to an input of both the driver and the output stages, and feeding the bias reduction signal to an input of the driver stage.

According to a second aspect of the present invention there is provided an electrical circuit comprising a power amplifier, an external control loop and a

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protection circuit; wherein the protection circuit comprises detection means for detecting an electrical parameter at an output of the power amplifier, bias reduction means for providing a bias signal at an input of the power amplifier and a reference signal generator coupled to the bias reduction means.

The power amplification circuit as described above can be utilised in a mobile telecommunications device.

Advantageously, the present invention mitigates problems associated with output power control in the prior art. Also, low voltage transistors (and other low voltage technologies) can be used and the invention be implemented on an integrated circuit using a minimum of components. Where high output mismatch conditions result in the circuit experiencing a high VSWR, the present invention functions to reduce the circuit output power variation.

Further advantage is obtained in that both the driver transistor and output transistor are protected from excessive voltage levels.

It is emphasised that the term 'comprises' or 'comprising' is used in this specification to specify the presence of stated features, integers, steps or components, but does not preclude the addition of one or more further features, integers, steps or components, or groups thereof.

Brief Description of the Drawings

Figure 1 is a schematic diagram of a RF power amplifier;

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Figure 2 is a schematic diagram of a RF power amplifier in accordance with an embodiment of the invention;

Figure 3 is a schematic diagram showing the RF power amplifier of Figure 2 in greater detail; and

Figure 4 is a flow chart showing the operational stages of the present invention.

Detailed Description of the Embodiments

Figure 1 illustrates a RF power amplifier 10, in which a RF signal 12 is input to a driver transistor 14. The collector electrode of the driver transistor 14 is coupled to a capacitor 16, which, in turn is coupled to an output transistor 20. An output bias circuitry 18 is coupled to the base electrode of the output transistor 20. Finally, the collector electrode of the output transistor 20 is coupled to a RF load 22. Generally, the RF load 22 is an antenna.

In operation, the RF signal 12 is amplified by the driver transistor 14, and the capacitor 16 serves to remove any d.c. component (leaving only the a.c. component) of the amplified signal before it is input to the output transistor 20. An approximately constant bias current is output from the output bias circuitry 18 and functions to bias the output transistor 20 such that the output transistor collector current is controlled.

The capacitor 16 functions to match impedance in the circuit and can be replaced by any suitable impedance matching element.

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In Figure 2, a RF power amplifier is coupled to an external control loop and a protection circuit. Specifically, in the RF power amplifier a RF signal 32 is input to a driver transistor 34. The collector electrode of the driver transistor 34 is coupled to a capacitor 36 which, in turn is coupled to an output transistor 38. A collector electrode of the output transistor 38 is coupled to a RF load 40 (which is generally an antenna).

Alternatively, the capacitor 36 can be replaced by other suitable RF matching means (such as a capacitor and shunt element in series or a transformer) as determined by the impedance transfer characteristics required within the RF power amplifier.

The external control loop includes a d.c. current detector 42 which is connected to the RF power amplifier at the collector electrode of both the driver transistor 34 and the output transistor 38. The d.c. current detector 42 and a reference current 46 are coupled to a regulator 44, which regulator 44 is coupled to a bias control signal generator 48. The external control loop further comprises a connection from the bias control signal generator 48 to each of the base electrode of the driver transistor 34 and the base electrode of the output transistor 38.

The protection circuit comprises a voltage envelope detector 50 and a protection level reference 52 both coupled to a bias reduction circuit 54. The voltage envelope detector 50 is connected to the collector electrode of the output transistor 38 and also, the bias reduction circuit 54 is connected to the base electrode of the driver transistor 34.

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In operation, the RF power amplifier functions in a similar manner to the RF power amplifier 10 of Figure 1. The d.c. current detector 42 detects any voltage swing (resulting from an impedance variation on the RF load 40) at the collector electrode of the output transistor 38.

The d.c. current detector 42 detects the d.c. current at the collector electrode of the output transistor 38. Generally, any alteration in this current is caused by an impedance variation on the RF load 40. The detected current is output from the d.c. current detector 42 and fed to the regulator 44 which processes the detected current in combination with the reference current 46. Where the detected current is lower than a predetermined threshold the regulator 44 produces a higher regulated output current and when the detected current is higher than a predetermined threshold the regulator 44 produces a lower regulated output current. The regulated output current is fed to the bias control signal generator 48 which provides a suitable bias current to the driver transistor 34 and the output transistor 38 to compensate for any impedance variation on the RF load 40.

The voltage envelope detector 50 detects the voltage envelope at the collector electrode of the output transistor 38. This signal is processed, in combination with a protection level reference signal 52, in the bias reduction circuit 54. The resulting signal is fed to the base electrode of the driver transistor 34 to ensure that a voltage swing at the output transistor 38 does not reach an excessive level.

Figure 3 illustrates the RF power amplifier of Figure 2 in greater detail, but common reference numerals are

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employed where common elements are illustrated. Specifically, additional detail can be found where a first choke element 35 and a second choke element 39 are coupled between the d.c. current detector 42 and the driver transistor 34 and the output transistor 38, respectively.

In the external control loop, the d.c. current detector 42 includes a resistor 420 connected to the input line from the regulator 44. The regulator 44 is shown to include a resistor 440 and an AND gate 441.

In the protection circuit, the voltage envelope detector 50 includes a diode 500 and a first resistor 501 connected in series. A capacitor 502 is coupled between the output of the diode 500 and ground, and a second resistor 503 is coupled between the output of the first resistor 501 and ground. The protection level reference 52 includes a resistor 520 coupled between ground and the protection level reference output. This output is connected to an emitter electrode of a transistor 540 located within the bias reduction circuit 54. Additionally, a first resistor block 56 connected to the base electrode of driver transistor 34 and a second resistor block 58 connected to the base electrode of output transistor 38, are illustrated.

The operation of the circuit of Figure 3 is described above, in relation to Figure 2.

As shown in Figure 4, the first stages of operation of the present invention involve the detection 60 62 of two parameters (namely the d.c. current and the voltage envelope) at the collector electrode of the output transistor. The detected d.c. current is regulated 64

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with respect to a reference current and then a bias control signal is generated 66 utilising the regulated signal. A control loop is completed when the bias control signal is fed 68 70 to the base electrode of each of the output transistor and the driver transistor.

Returning to the detected voltage envelope, a bias signal is generated 72 utilising the detected voltage envelope with respect to a reference voltage. A protection function is performed when the bias reduction signal is fed 70 to a base electrode of the driver transistor. Both the control loop function and the protection function are performed on a continuous basis during the operation of the RF power amplifier.

It will be apparent to the skilled person that the above described circuit architecture is not exhaustive and variations on this structure may be employed to achieve a similar result whilst employing the same inventive concept.

It can therefore be seen that the present invention provides a power amplification circuit which has significant advantages over conventional devices.

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Claims

1. A method of controlling output from a power amplifier which has a driver stage and an output stage, the method comprising:

detecting a first and a second electrical parameter at an output of the output stage;

processing the first parameter with a first reference signal to generate a bias control signal;

processing the second parameter with a second reference signal to generate a bias reduction signal;

feeding the bias control signal to an input of both the driver and the output stages;

feeding the bias reduction signal to an input of the driver stage.

2. The method of controlling output from a power amplifier as claimed in claim 1, wherein the first electrical parameter is an electrical current.

3. The method of controlling output from a power amplifier as claimed in claim 1, wherein the second electrical parameter is an output voltage envelope.

4. An electrical circuit comprising:

a power amplifier, an external control loop and a protection circuit; wherein the protection circuit comprises:

detection means for detecting an electrical parameter at an output of the power amplifier;

bias reduction means for providing a bias signal at an input of the power amplifier;

a reference signal generator coupled to the bias reduction means.

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5. The electrical circuit of claim 4, wherein the power amplifier has a driver stage and an output stage.

6. The electrical circuit of claim 5, wherein the detection means is coupled to the output of the output stage.

7. The electrical circuit of claim 6, wherein the bias reduction means is coupled to the input of the driver stage.

8. A mobile telecommunications device including the power amplification circuit as claimed in claims 4 to 7.

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Abstract

Circuit for power amplification

A radio frequency (RF) power amplifier, including an external control loop and a protection circuit, which functions to maintain a constant output power during variations in impedance on the RF load. In the external control loop a collector current from an output transistor is detected and then regulated with respect to a reference current. The regulated signal is utilised to generate a bias control signal which is input to the base electrode of both a driver transistor and the output transistor. The protection circuit detects a voltage envelope at the collector electrode of the output transistor and utilises this signal to form a bias reduction signal which is input to the base electrode of the driver transistor.

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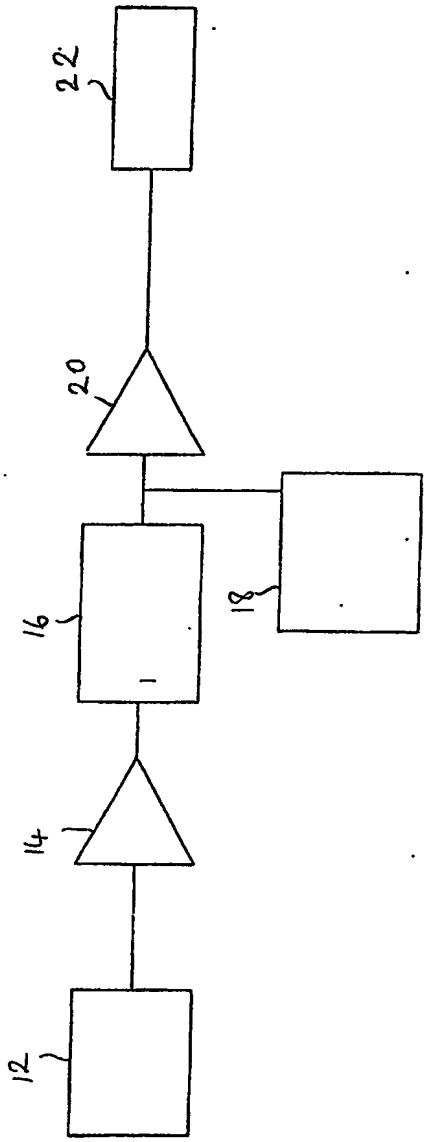


FIG. 1

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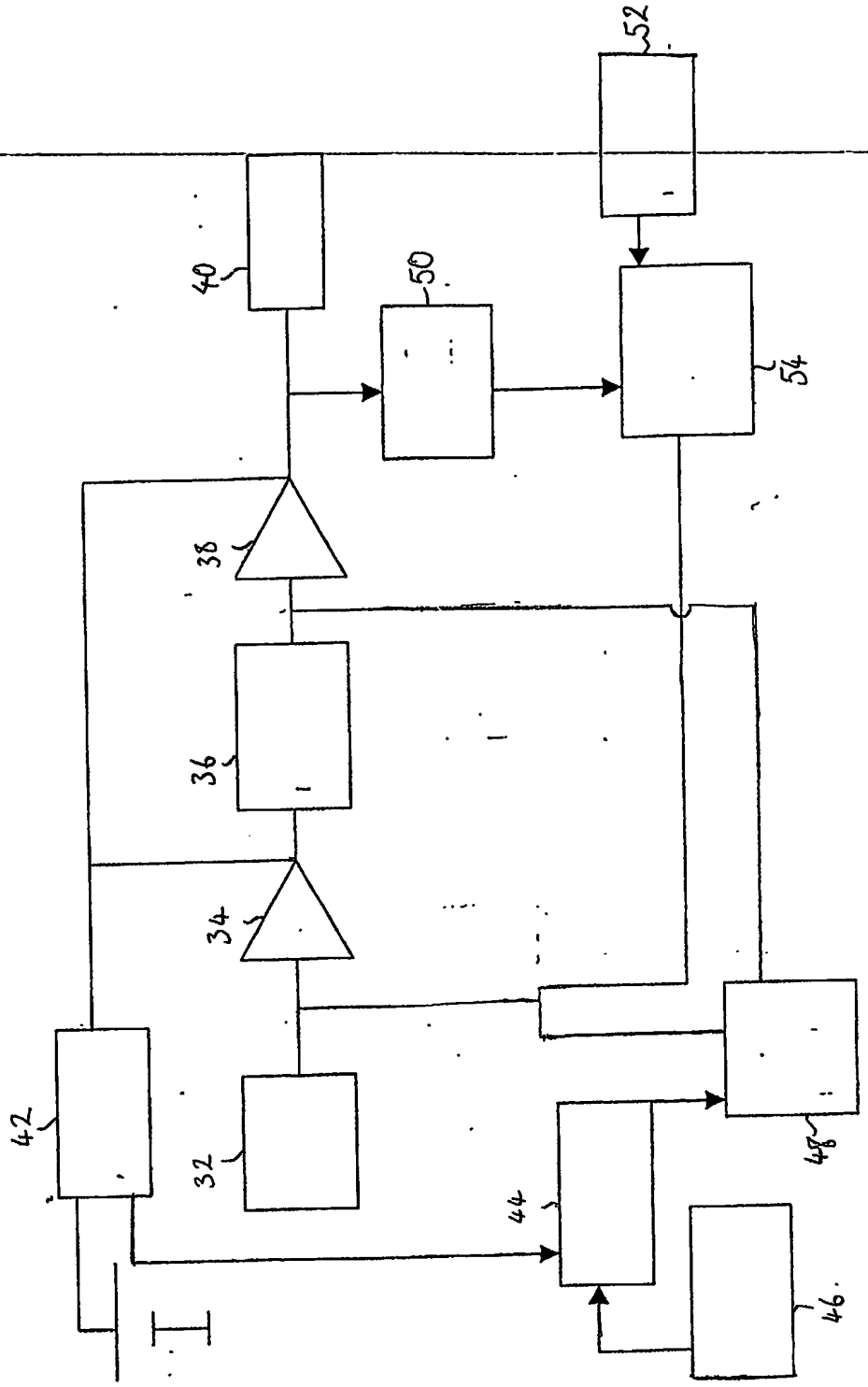


FIG. 2

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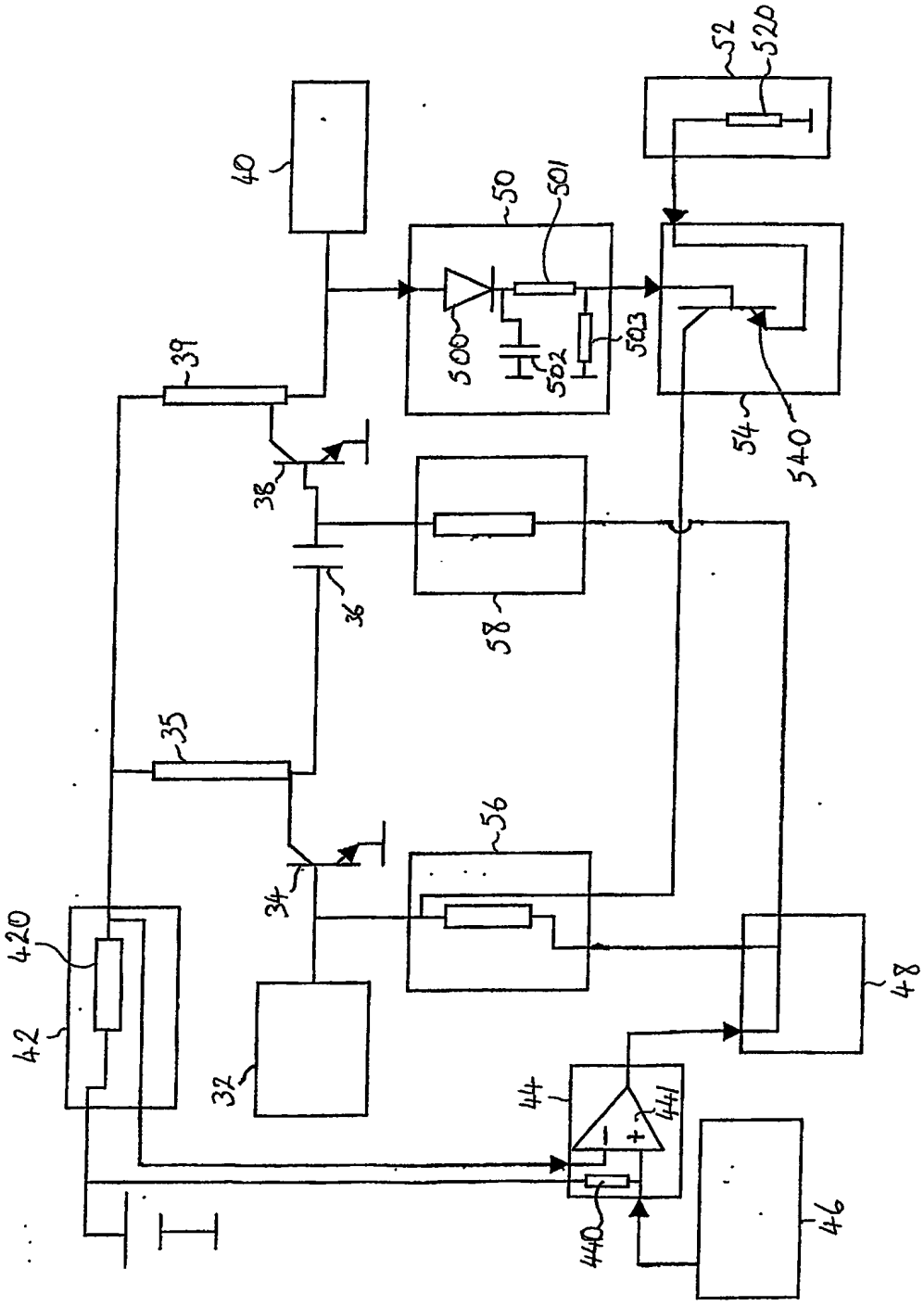


FIG. 3

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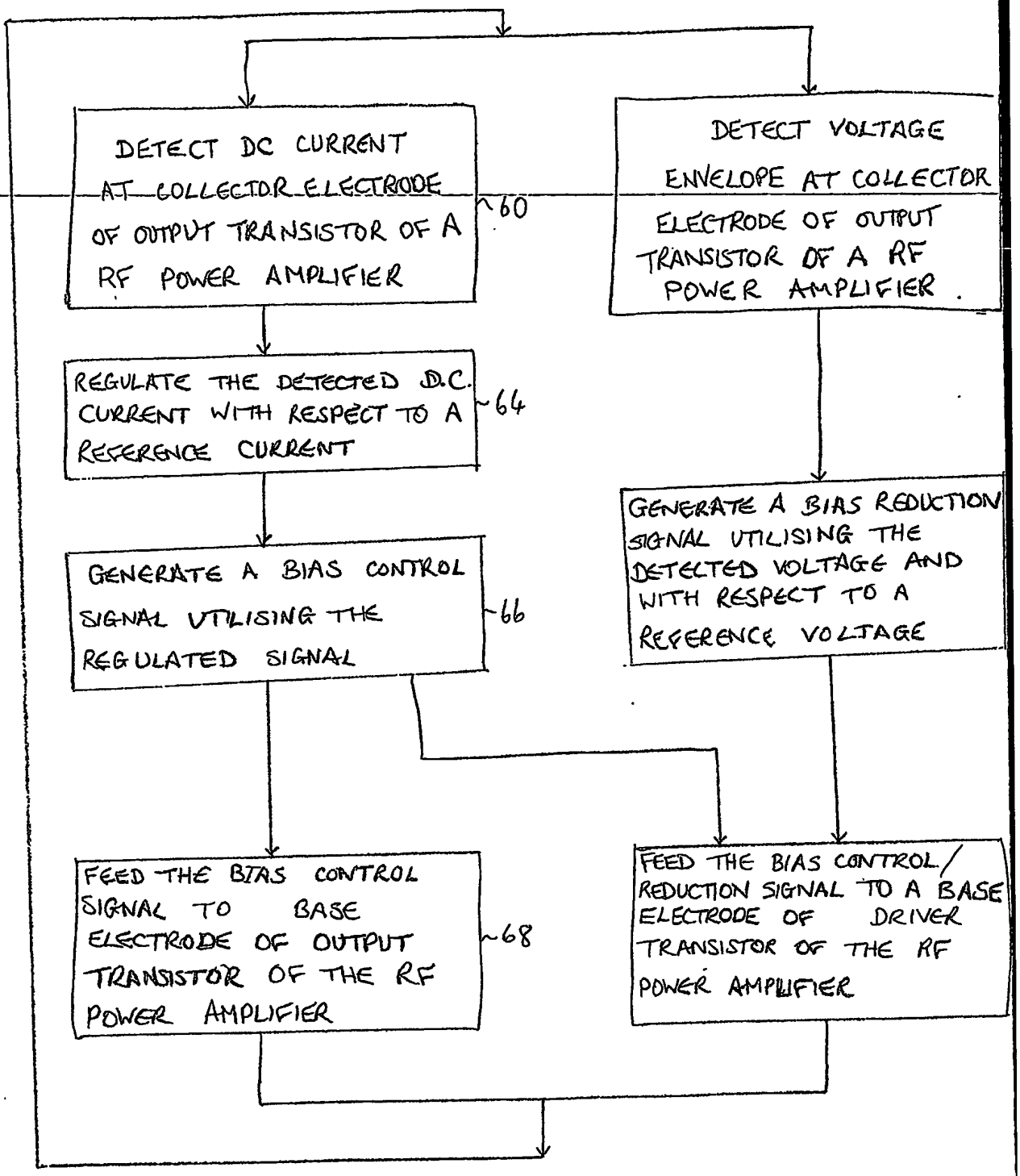


FIG. 4

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